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PATENT APPLICATION

POWER DEVICE WITH BI-DIRECTIONAL LEVEL SHIFT CIRCUIT

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CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of U.S. Patent Application No. 10/349,804, filed on January 22, 2003, which claims priority to U.S. Provisional Patent Application No. 60/354,701, filed on February 4, 2002, both of which are incorporated by reference herein for all purposes.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a gate driver having level shift circuit for driving the gate of a power semiconductor device.

[0003] Many low voltage electronic circuits, e.g., MOSFET devices, are used to drive high voltage switching transistors, e.g., power MOSFETs, insulated gate bipolar transistor devices (IGBTs), gate controlled thyristors, and the like. A power semiconductor switch or device is switched from a nonconducting state to a conducting state by raising the gate-source voltage from below to above a threshold voltage. As used herein, the term "power device" or "power semiconductor device" refers to any power MOSFET, IGBT, thyristor, or the like.

[0004] One or more low voltage transistors, coupled to an output node of the gate driver, apply appropriate voltages to the gate or control terminal of the power device to turn on or turn off the power device. When the power device is an N-channel metal oxide semiconductor field effect transistor (NMOSFET), the device is turned on by applying a high voltage to the gate of the power switch and turned off by applying a low voltage to the gate. In contrast, if the power device is a P-channel metal oxide semiconductor field effect transistor (PMOSFET), the device is turned on by applying a low voltage to the gate of the power switch and turned off by applying a high voltage to the gate. Unless otherwise explained, power devices, as used herein, refer to in N type devices for ease of illustration.

[0005] Generally, a gate driver includes a level shifting circuit for shifting the potential of a small control signal to a higher voltage level that is more suitable for turning on the power device. The gate driver may be packaged as a single device having a high side portion and a low side portion, where the high side is used to turn on or off a high side switch or transistor of the power device and the low side is used to turn on or off a low side switch or transistor

of the power device. The high side switch has a drain coupled to a high voltage source, e.g., 1000 volts, while the low side switch has a drain coupled to a lower voltage source, e.g., a source of the high side switch.

BRIEF SUMMARY OF THE INVENTION

[0006] In one embodiment, a power module includes a power semiconductor device having a first terminal, a second terminal, and a third terminal. The second terminal is a control terminal to regulate flow of electricity between the first and third terminals. A gate driver has an output node coupled to the second terminal of the power device to provide gate control signals to the power semiconductor device. The gate driver includes a gate control signal generator having a first input and a second input and a first sub-circuit having a first signal path and a second signal path that are suitable for transmitting signals. The first and second signal paths are coupled to the first input of the gate control signal generator. The second signal path is configured to provide a signal to the first input with a reduced signal delay. The gate driver further includes a second sub-circuit coupled to the second input of the gate control signal generator.

[0007] In another embodiment, a gate driver includes a gate control signal generator having a first input and configured to output a gate control signal to a power semiconductor switch and a first sub-circuit having a first signal path and a second signal path that are suitable for transmitting signals. The first and second signal paths are coupled to the first input of the gate control signal generator. The second signal path is configured to provide a signal to the first input with a reduced signal delay.

[0008] In yet another embodiment, a power device includes a gate control signal generator having a first input and configured to output a gate control signal to a power semiconductor switch. A first sub-circuit has a first signal path and a second signal path that are suitable for transmitting signals. The first and second signal paths are coupled to the first input of the gate control signal generator. The second signal path is configured to provide a signal to the first input with a reduced signal delay. A second sub-circuit includes a third signal path and a fourth signal path that are suitable for transmitting signals. The third and fourth signal paths are coupled to the second input of the gate control signal generator. The first input of the gate control signal generator receives a signal of first voltage from the first sub-circuit and the second input of the gate control signal generator receives a signal of second voltage from

the second sub-circuit. The gate control signal generator outputs a gate control signal according to a voltage difference between the signal of first voltage and the signal of second voltage. The second signal path and fourth signal path are feed forward connections.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 illustrates a schematic diagram of a power module according to one embodiment of the present invention.

[0010] Fig. 2 illustrates a schematic diagram of a gate driver according to one embodiment of the present invention.

[0011] Fig. 3 illustrates a schematic circuit diagram of a signal generator having a level shift circuit according to one embodiment of the present invention.

[0012] Fig. 4A illustrates a schematic, partially delayered top structural view of a sub-circuit of the level shift circuit according to one embodiment of the present invention.

[0013] Fig. 4B illustrates a cross-sectional view of the structure of Fig. 4A taken along the arrows AA according to one embodiment of the present invention.

[0014] Fig. 5 illustrates a schematic circuit diagram of a signal generator having a level shift circuit with two sub-circuits in series according to one embodiment of the present invention.

[0015] Fig. 6A illustrates a schematic, partially delayered top structural view of the two sub-circuits of the level shift circuit of Fig. 5 according to one embodiment of the present invention.

[0016] Fig. 6B illustrates a cross-sectional view of the structure of Fig. 6A taken along the arrows BB according to one embodiment of the present invention.

[0017] Fig. 7A illustrates a cross-sectional view of a partially fabricated substrate having a conductive region that extends from a metal layer to a bonding pad according to one embodiment of the present invention.

[0018] Fig. 7B illustrates a cross-sectional view of the substrate of Fig. 7A having a first dielectric layer and a trench according to one embodiment of the present invention.

[0019] Fig. 7C illustrates a cross-sectional view of the substrate of Fig. 7B having a resistor formed overlying the conductive region according to one embodiment of the present invention.

[0020] Fig. 8 illustrates a bi-directional level shift circuit according to one embodiment of the present embodiment.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Fig. 1 schematically illustrates a power module 100 according to one embodiment of the present invention. The power module includes a first power device or gate driver 102 having a high side driver 104 and a low side driver 106, a second power device or switch 108 having a high side transistor 110 and a low side transistor 112, and a signal provider or pulse width modulation (PWM) controller 114.

[0022] The second power device 108 has a half bridge configuration. The drain is coupled to a high voltage source, e.g., 1,000 volts, and its source is coupled to the drain of the low side transistor. The source of the low side transistor, in turn, is grounded. In another embodiment, the drain and source of the high side transistor are coupled to a positive voltage source, e.g., 500 volts, and a negative voltage source, e.g., -500 volts.

[0023] The power device 108 includes an output node 114 coupled to a node between the source of the high side transistor 110 and the drain of the low side transistor 112. The output node is coupled to and provides an output voltage signal to drive an external load. As shown, the high side driver 104 and the low side driver 106 provide a high-side gate control signal HG and a low-side gate control signal LG to the gate electrode of the high side transistor 110 and the gate electrode of the low side transistor 112, respectively. A feed back signal HS from the source of the high side transistor 110 is provided to the high side driver 104 for use by the high side driver in generating the high-side control signal HG.

[0024] Referring to Figs. 1 and 2, the PWM controller 114 provides a high-side signal HC and a low-side signal LC that are used by the high side driver and the low side driver, respectively, to generate the high-side gate control signal HG and the low-side gate control signal LG. A transceiver 202 in the low side driver receives the high-side signal HC and transmits appropriate one or more signals to a high side receiver 204 provided in the high side driver. The high side receiver 204 transmits a signal to a circuit 206 in the high side driver

that, in turn, provides the high-side gate control signal HG to the gate electrode of the high side transistor 110. A low side receiver 208 receives the low-side signal LC and transmits a signal to a circuit 210 that, in turn, provides the low-side gate control signal LG to the gate electrode of the low side transistor 112. In one embodiment, the high side driver does not include the circuit 206. That is, the signal output from the receiver 204 is applied directly to the gate electrode of the high side transistor.

[0025] In operation, the high side transistor is turned on and the low side transistor is turned off to provide a high output voltage V_{out} via the output node. On the other hand, the high side transistor is turned off and the low side transistor is turned on to provide a low output voltage V_{out} via the output node.

[0026] A delay circuit may be provided in the low side driver 106, e.g., in the circuit 210, to ensure that the low side transistor 112 is not turned on while the high side transistor is turned on. That is, the delay circuit provides a dead time between the turn-on time of the high side transistor and the turn-on time of the low side transistor to prevent cross conduction. The delay circuit may use a plurality of inverters in series to obtain the desired signal delay, as explained in more detail in a patent application entitled, "Efficient Gate Driver IC for Power Devices," filed on April 30, 2002, assigned to the present assignee (Attorney Docket: 011775-011210US), which is incorporated by reference herein for all purposes.

[0027] In one embodiment, a level shift circuit and related components described herein below are provided within a signal generator 208 that includes the transceiver 202 and the receiver 204. The signal generator 208 is distributed in the high and low side drivers 104 and 106 in the present embodiment. In other embodiments, the signal generator 208 is provided entirely in the high side driver.

[0028] Fig. 3 depicts a signal generator 300 including a resistive level shift circuit 302 according to one embodiment of the present invention. A dotted line 304 indicates whether varies components in the signal generator is provided in the high side driver or the low side driver. The placement of these components in the high side or low side driver is embodiment specific. For example, in the present embodiment, the level shift circuit 302 is distributed between the high and low side drivers. However, the level shift circuit may be provided entirely in the high side driver.

[0029] The signal generator 300 includes a first voltage source 306 and a pulse generator 308 that are coupled to a plurality of inverters 310, 312, and 314. The inverters are arranged serially into two different groups. The first group includes the inverters 310 and 312, and the second group includes the inverter 314. The inverters in the first and second groups are configured to output complementary signals to the level shift circuit 302. That is, the first group outputs a first signal V1, and the second group outputs a second signal V1' that is complementary to the signal V1.

[0030] A first sub-circuit 316 of the level shift circuit 302 receives the first signal V1. The first sub-circuit 316 includes a resistor R1, a capacitor C1, and a capacitor Cs. A first node 318 of the resistor R1 is coupled to the output of the first group of invertors. A second node 320 of the resistor R1 outputs a first voltage that is used to generate a gate control signal, as explained in more detail later. The capacitor C1 represents the resistor-to-substrate capacitance. On the other hand, the capacitor Cs represents the bond pad-to-substrate capacitance. A first node 322 (e.g., substrate) of the capacitor Cs is coupled to the first node 318 of the resistor R1, and the second node 324 (e.g., bond pad) of the capacitor Cs is coupled to the second node 320 of the resistor R1. As used herein, the term "substrate" includes a conductive layer, such as an N diffusion layer, formed on the substrate.

[0031] In one embodiment, the capacitor Cs is formed by providing a conductive layer below a bonding pad and on an upper surface of the semiconductor substrate, as explained in greater detail subsequently. The conductive layer is configured to extend below the resistor R1 and is electrically coupled to the first node of the resistor R1. Accordingly, the second node 324 of the capacitor Cs is commonly shared with the capacitor C1. That is, the capacitors C1 and Cs are provided with return points. A feed forward connection 326 provided by the capacitor Cs and its nodes 322 and 324 enhances the device performance by preventing a lag or pole (signal delay) from being introduced to the edges of a signal. Without the feed forward connection, i.e., the conductive layer, the capacitor C1 would represent a stray resistor-to-substrate capacitance that would degrade the device performance.

[0032] Similarly, a second sub-circuit 328 of the level shift circuit 302 receives the second, complementary signal V1'. The second sub-circuit 328 includes a resistor R1a, a capacitor C1a, and a capacitor Csa. A first node 330 of the resistor R1a is coupled to the output of the second inverter group. A second node 332 of the resistor R1a outputs a second voltage that is used to generate a gate control signal. The capacitor C1a represents the resistor-to-substrate

capacitance. The capacitor Csa represents the pad metal-to-substrate capacitance. A first node 334 of the capacitor Csa is coupled to the first node 330 of the resistor R1a, and a second node 336 of the capacitor Csa is coupled to the second node 332 of the resistor R1a.

[0033] The capacitor Csa is formed by providing a conductive layer below a bonding pad and on an upper surface of the semiconductor substrate. The conductive layer is configured to extend below the resistor R1a and is electrically coupled to the first node of the resistor R1a. Accordingly, the second node of the capacitor Csa is commonly shared with the capacitor C1a. A feed forward connection 336 is provided by the capacitor Csa, and its nodes 332 and 334 enhance the device performance, as explained above.

[0034] The level shift circuit 302 includes a hysteresis comparator 338 (or gate control signal generator) having a first input 340, a second input 342, and an output 344. The first input is coupled to the node 320 of the resistor R1 that outputs a first voltage, and the second input is coupled to the node 332 of the resistor R1a that outputs a second voltage that is complementary of the first voltage. Capacitors C2 and C2a are associated with the first input 340 and the second input 342. A voltage difference V2 between the first voltage and the second voltage is used to drive the comparator and output a high-side gate control signal HG via the output node 344.

[0035] The level shift circuit 302 further includes a first capacitor-resistor network 346 and a second capacitor-resistor network 348. An input node 350 of the first capacitor-resistor network is coupled to the output of the first sub-circuit. The first capacitor-resistor includes a resistor R2, a resistor R3, and a capacitor C3. The resistors R2 and R3 are provided in a parallel configuration and coupled to the output of the first sub-circuit. The capacitor C3 is provided in series with the resistor R3 and coupled to a second voltage source 352. The voltage source 352 is also coupled to one end of the resistor R2.

[0036] Similarly, an input node 354 of the second capacitor-resistor network is coupled to the output of the second sub-circuit. The second capacitor-resistor network includes a resistor R2a, a resistor R3a, and a capacitor C3a. The resistors R2a and R3a are provided in a parallel configuration and coupled to the output of the second sub-circuit. The capacitor C3a is provided in series with the resistor R3a and coupled to the second voltage source 352. The voltage source 352 is also coupled to one end of the resistor R2a.

[0037] In one embodiment, the values of the capacitors C2, C2a, C3, C3a and the resisters R2, R2a, R3, and R3a are selectively provided to prevent voltage spikes that may be

generated by the feed forward connections 326 and 328. The level shift circuit 302 has been provided with the following values to obtain attenuation of 50:1:

C2 = 50 pf
C2a = 50 pf
C3 = 5 pf
C3a = 5 pf
R2 = 20,000 ohms
R2a = 20,000 ohms
R3 = 10,000 ohms
R3a = 10,000 ohms

[0038] If a greater attenuation ratio is desired, the values of the capacitors may be increased and the values of the resistors may be decreased. On the other hand, if a lower attenuation ratio is desired, the values of the capacitors may be decreased and the values of the resistors may be increased.

[0039] Fig. 4A illustrates a schematic, partially delayered, structural top view 400 of the first sub-circuit 316 of the level shift circuit 302 according to one embodiment of the present invention. The structure 400 depicts a conductive layer 402 provided on an upper surface of a substrate (not shown), a bond pad 404 overlying a portion of the conductive layer, the resistor R1, a wire 406 corresponding to the node 320 in Fig. 3 that is bonded to the bond pad 404, and a metallization layer 408 corresponding to the node 318 in Fig. 3. The resister R1 is coupled to the wire 406 and the metallization layer 408 via contacts 410 and 412, respectively. A contact 414 electrically couples the metallization layer 408 and the conductive layer 402 to provide the feed forward connection 326 of Fig. 3. The conductive layer 402 is an N diffusion region in one embodiment. The conductive layer 402 extends below the resistor R1 and the bond pad 404 to provide the capacitors C1 and Cs.

[0040] Fig. 4B illustrates a schematic, cross-sectional view of the structure 400 taken along the arrows AA according to one embodiment of the present invention. The structure 400 depicts a substrate 416, the conductive layer 402, the bond pad 404, the wire 406, the metallization layer 408, the contacts 410, 412, and 414, and the resister R1. The structure

400 further includes a dielectric layer 418 provided over the conductive layer 402 to separate the conductive layer from the resistor R1 and the bond pad 404. The dielectric layer 418, accordingly, provides the capacitors C1 and Cs.

[0041] In one embodiment, the dielectric layer 418 is an oxide layer. The thickness of the oxide layer below the bond pad is about 10,000 angstroms, and the thickness of the oxide layer below the resistor R1 is about 6,000 angstroms. The breakdown voltage of the oxide layer is generally 70 volts/1000 angstroms. The breakdown voltage of the structure 400 or the level shift circuit 302, accordingly, is about 420 volts for the above design specification. Increasing the oxide layer thickness may raise the breakdown voltage.

[0042] Fig. 5 illustrates an alternative method of increasing the break down voltage according to one embodiment of the present invention. A signal generator 500 includes a level shift circuit 502 having a first sub-circuit 504, a second sub-circuit 506, a first capacitor-resistor network 508, a second capacitor-resistor network 510, a third sub-circuit 512, and a fourth sub-circuit 514. The first and second sub-circuits 504 and 506 correspond to the first and second sub-circuits 316 and 328 of the level shift circuit 302. The first and second capacitor-resistor network 508 and 510 correspond to the first and second capacitor-resistor network 346 and 348 of the level shift circuit 302.

[0043] The first sub-circuit 504 includes a resistor R1, a capacitor C1, and a capacitor Cs. A first node of the resistor R1 or input of the first sub-circuit 504 receives a voltage signal V1 from an output of a group of invertors. A second node 518 of the resistor R1 or output of the first sub-circuit 504 outputs a first voltage that is used subsequently to generate a gate control signal, as in the level shift circuit 302. The capacitor C1 represents the resistor-to-substrate capacitance. The capacitor Cs represents the bond pad-to-substrate capacitance. A first node 522 (e.g., substrate) of the capacitor Cs is coupled to the first node 516 of the resistor R1, and the second node 524 (e.g., bond pad) of the capacitor Cs is coupled to the second node 518 of the resistor R1. The second sub-circuit 506 has substantially the same configuration as the first sub-circuit 504.

[0044] The third and fourth sub-circuits 512 and 514 have similar configuration as the first and second sub-circuits 504 and 506. The third sub-circuit 512 includes a resistor R4, a capacitor C4, and a capacitor Csb. A first node 526 of the resistor R4 or input of the third sub-circuit 512 is coupled to the output of the first sub-circuit 504. A second node 528 of the resistor R4 or output of the third sub-circuit 512 is coupled to an input of a comparator 530.

The capacitor C4 represents the resistor-to-substrate capacitance. The capacitor Csb represents the bond pad-to-substrate capacitance. A first node 532 (e.g., bond pad) of the capacitor Csb is coupled to the first node 526 of the resistor R4, and the second node 534 (e.g., substrate) of the capacitor Csb is coupled to the second node 528 of the resistor R4. The fourth sub-circuit 514 has substantially the same configuration as the third sub-circuit 512.

[0045] Accordingly, the third and fourth sub-circuits 512 and 514 are provided in series with the first and second sub-circuits 504 and 506, respectively. The first and second sub-circuits 504 and 506 have feed forward connections 536 and 538, respectively, to enhance device performance. The third and fourth sub-circuits 512 and 514 similarly have feed forward connections 540 and 542, respectively, to enhance device performance. In one embodiment, the first and second sub-circuits 504 and 506 are provided in the low side driver, and the third and fourth sub-circuits 512 and 514 are provided in high side driver.

[0046] As with the first sub-circuit 316, the first sub-circuit 504 of the level shift circuit 502 has a breakdown voltage of about 420 volts. In addition, the third sub-circuit 512 provided in series with the first sub-circuit has a breakdown voltage of about 420 volts. Accordingly, the level shift circuit 502 is provided with a breakdown voltage of about 840 volts. An additional sub-circuit may be provided in series with the first and third sub-circuits to provide a higher breakdown voltage.

[0047] Figs. 6A illustrates a schematic, partially delayered, structural top view 600 of the first sub-circuit 504 of the level shift circuit 502 and a schematic, partially delayered, structural top view 602 of the third sub-circuit 512 according to one embodiment of the present invention. The structure 600 and the structure 602 are provided in the low side driver and the high side driver, respectively.

[0048] The structure 600 depicts a conductive layer 606 provided on an upper surface of a substrate (not shown), a bond pad 608 overlying a portion of the conductive layer, the resistor R1, a wire 610 that is bonded to the bond pad 608, and a metallization layer 612. The resistor R1 is coupled to the wire 610 and the metallization layer 612 via contacts 614 and 616, respectively. A contact 616 electrically couples the metallization layer 612 and the conductive layer 606 to provide the feed forward connection 536. The conductive layer 606 extends below the resistor R1 and the bond pad 608 to provide the capacitors C1 and Cs. The conductive layer 606 is an N diffusion region in one embodiment.

[0049] The structure 602 depicts a conductive layer 618 provided on an upper surface of a substrate (not shown), a bond pad 620 overlying a portion of the conductive layer, the resistor R4, a wire 622 that is bonded to the bond pad 620, and a metallization layer 624. The wire 622 is coupled to the wire 610 of the structure 600. The resistor R4 is coupled to the wire 622 and the metallization layer 624 via contacts 626 and 628, respectively. A contact 630 electrically couples the metallization layer 624 and the conductive layer 618 to provide the feed forward connection 540. The conductive layer 618 extends below the resistor R4 and the bond pad 620 to provide the capacitors C4 and Csb.

[0050] Fig. 6B illustrates a schematic, cross-sectional view of the structures 600 and 602 taken along the arrows BB according to one embodiment of the present invention. The structure 600 depicts a substrate 632, the conductive layer 606, the bond pad 608, the wire 610, the metallization layer 612, the contacts 614, and 616, and the resister R1. The structure 600 further includes a dielectric layer 634 provided over the conductive layer 606 to separate the conductive layer from the resistor R1 and the bond pad 608. The resistor R1, the bond pad 608, and the dielectric layer 634 together form the capacitors C1 and Cs.

[0051] Similarly, the structure 602 depicts the substrate 632, the conductive layer 618, the bond pad 620, the wire 622, the metallization layer 624, the contacts 626 and 628, and the resister R4. The structure 602 further includes a dielectric layer 636 provided over the conductive layer 618 to separate the conductive layer from the resistor R4 and the bond pad 620. The resistor R4, the bond pad 620, and the dielectric layer 636 together form the capacitors C4 and Csb.

[0052] In one embodiment, the dielectric layer 634 is an oxide layer. The thickness of the oxide layer below the bond pad is about 10,000 angstroms and below the resistor R1 is about 6,000 angstroms. The breakdown voltage of the oxide layer is generally 70 volts/1000 angstroms. The breakdown voltage of the structure 600, accordingly, is about 420 volts for the above design specification. Similarly, the dielectric layer 636 is an oxide layer having a thickness below the bond pad of about 10,000 angstroms and a thickness below the resistor R4 of about 6,000 angstroms. The breakdown voltage of the structure, accordingly, is about 420 volts for the above design specification. The structures 600 and 602 together provide the level shift circuit 502 with a breakdown voltage of 840 volts.

[0053] Fig. 7A illustrates a cross-sectional view of a substrate 702 that has been partially fabricated to provide thereon a circuit corresponding to the first sub-circuit 316 of Fig. 4B

according to one embodiment of the present invention. The substrate 702 is a semiconductor, e.g., silicon substrate. A conductive region 704, e.g., N diffusion region, is formed on an upper surface of the substrate 702. In one embodiment, N type dopants are injected into the substrate using an ion implantation method. Thereafter, the dopants are diffused to form the conductive region 704.

[0054] A first dielectric layer 706, e.g., oxide layer, is formed overlying the conductive layer 704 to a first thickness (Fig. 7B). A first photoresist (not shown) is provided over the first dielectric layer 706 and patterned to expose an area 708. The exposed area 708 is etched to form a trench 709. The trench 709 overlies the conductive layer 706 without contacting the conductive layer, so that the these two regions are electrically isolated. The first photoresist is stripped from the substrate using a conventional technique.

[0055] A conductive layer 728, e.g., polysilicon, is deposited within the trench 709 (Fig. 7C). The conductive layer 728 is patterned to form a resistor corresponding to the resistor R1 of Figs. 3 and 4A. Thereafter, a second dielectric layer 710, e.g., oxide layer, is formed over the patterned conductive layer and the first dielectric layer. A second photoresist (not shown) is provided over the second dielectric layer and patterned to expose portions 714, 716, and 718 of the second dielectric layer. The exposed portions are etched to form a plurality of trenches 715, 717, and 719. The second photoresist is stripped away using a conventional technique. The trenches 715, 717, and 719 are filled with conductive material to form a plurality of plugs corresponding to the contacts 410, 412, and 414 of Fig. 4A. Thereafter, the fabrication process continues to provide the substrate 702 with a bonding pad and wiring, as shown in Fig. 4A. The plug formed within the trench 719 that is electrically coupled to the conductive region 704 and the conductive region 704 provided below the bonding pad to form a capacitor Cs together provide a feed forward connection to enhance device performance according to one embodiment of the present invention.

[0056] Fig. 8 depicts a signal generator 1000 including a bidirectional resistive level shift circuit 1002 according to one embodiment of the present invention. In the present embodiment,t the signal generator 100 is a module with at least two semiconductor dice. A dotted line 1004 indicates whether varies components in the signal generator is provided in a low side driver 1003a or a high side driver 1003b. The two drivers are coupled via wires 1005a and 1005b. That is, a first low-side node 1007a of the low side driver is coupled to a first high-side node 1009a of the high side driver via the wire 1005a, and the a second low-

side node 1007b of the low side driver is coupled to a second high-side node 1009b of the high side driver via the wire 1005b. These nodes serve as both input and output nodes in the present embodiment. Various components of the signal generator 1000 are described below in terms of their relationships to the high-side and low-side drivers; however, the placement of one or more of these components in the high-side or low-side driver is embodiment specific, as will be understood by those skilled in the art.

[0057] The signal generator 1000 includes a first voltage source 1006 and a first pulse generator 1008 that are coupled to a plurality of inverters 1010, 1012, and 1014. The inverters are arranged serially into two different groups. The first group includes the inverters 1010 and 1012, and the second group includes the inverter 1014. The inverters in the first and second groups are configured to output complementary signals to the level shift circuit 1002. That is, the first group outputs a first signal V1, and the second group outputs a second signal V1' that is complementary to the signal V1.

[0058] A first sub-circuit 1016 of the level shift circuit 1002 receives the first signal V1. The first sub-circuit 1016 includes a resistor R1, a capacitor C1, and a capacitor Cs. A first node 1018 of the resistor R1 is coupled to the output of the first group of invertors. A second node 1020 of the resistor R1 outputs a first voltage that is used to generate a gate control signal. The capacitor C1 represents the resistor-to-substrate capacitance. On the other hand, the capacitor Cs represents the bond-pad-to-substrate capacitance. A first node 1022 (e.g., substrate) of the capacitor Cs is coupled to the first node 1018 of the resistor R1, and a second node 1024 (e.g., bond pad) of the capacitor Cs is coupled to the second node 1020 of the resistor R1. The capacitor Cs is provided with a first potential V_{BVC1} according to one implementation.

[0059] A feed forward connection 1026 is provided to enhance the device performance by preventing a lag or pole (signal delay) from being introduced to the edges of a signal. Without the feed forward connection, i.e., the conductive layer, the capacitor C1 would represent a stray resistor-to-substrate capacitance that would degrade the device performance.

[0060] Similarly, a second sub-circuit 1028 of the level shift circuit 1002 receives the second, complementary signal V1'. The second sub-circuit 1028 includes a resistor R1a, a capacitor C1a, and a capacitor Csa. A first node 1030 of the resistor R1a is coupled to the output of the second inverter group. A second node 1032 of the resistor R1a outputs a second voltage that is used to generate a gate control signal. The capacitor C1a represents the

resistor-to-substrate capacitance. The capacitor Csa represents the pad metal-to-substrate capacitance. A first node 1034 of the capacitor Csa is coupled to the first node 1030 of the resistor R1a, and a second node 1036 of the capacitor Csa is coupled to the second node 1032 of the resistor R1a. A feed forward connection 1036 is provided to enhance the device performance. The capacitor Csa is provided with a second potential V_{BVCla} according to one implementation. The first potential V_{BVCl} and second potential V_{BVCla} are substantially the same.

[0061] The level shift circuit 1002 includes a hysteresis comparator 1038 (or gate control signal generator) having a first input 1040, a second input 1042, and an output 1044. The first input is coupled to the node 1020 of the resistor R1 that outputs a first voltage, and the second input is coupled to the node 1032 of the resistor R1a that outputs a second voltage that is complementary of the first voltage. Capacitors C2 and C2a are associated with the first input 1040 and the second input 1042. A voltage difference V2 between the first voltage and the second voltage is used to drive the comparator and output a high-side gate control signal HG via the output node 1044.

[0062] The level shift circuit 1002 further includes a first capacitor-resistor network 1046 and a second capacitor-resistor network 1048. An input node 1050 of the first capacitor-resistor network is coupled to the output of the first sub-circuit. The first capacitor-resistor includes a resistor R2, a resistor R3, and a capacitor C3. The resistors R2 and R3 are provided in a parallel configuration and coupled to the output of the first sub-circuit. The capacitor C3 is provided in series with the resistor R3 and coupled to a second voltage source 1052. The second voltage source 1052 defining a potential of V_{SF}. The voltage source 1052 is also coupled to one end of the resistor R2. A second pulse generator 1053 is coupled to the voltage source 1052 and inputs control signals to the comparator 1038. The second pulse generator 1053 defining a potential of V_{CM}. The voltage source 1052 and the pulse generator 1053 are provided external to the level shift circuit 1002 in the present embodiment.

[0063] Similarly, an input node 1054 of the second capacitor-resistor network is coupled to the output of the second sub-circuit. The second capacitor-resistor network includes a resistor R2a, a resistor R3a, and a capacitor C3a. The resistors R2a and R3a are provided in a parallel configuration and coupled to the output of the second sub-circuit. The capacitor C3a is provided in series with the resistor R3a and coupled to the second voltage source 1052. The voltage source 1052 is also coupled to one end of the resistor R2a.

[0064] In one embodiment, the values of the capacitors C2, C2a, C3, C3a and the resisters R2, R2a, R3, and R3a are selectively provided to prevent voltage spikes that may be generated by the feed forward connections 1026 and 1028. A desired attenuation may be obtained by selecting appropriate values for the capacitors and resistors, as explained above in connection with Fig. 3.

[0065] The level shift circuit 1002 also includes a third sub-circuit 1112 and a fourth sub-circuit 1114. The third sub-circuit 1112 includes a resistor R4, a capacitor C4, and a capacitor Csb. A first node 1126 of the resistor R4 or input of the third sub-circuit 1112 is coupled to the output of the first sub-circuit 1016. A second node 1128 of the resistor R4 or output of the third sub-circuit 1112 is coupled to an input of a comparator 1038. The capacitor C4 represents the resistor-to-substrate capacitance. The capacitor Csb represents the bond-pad-to-substrate capacitance. A first node 1132 (e.g., bond pad) of the capacitor Csb is coupled to the first node 1126 of the resistor R4, and the second node 1134 (e.g., substrate) of the capacitor Csb is coupled to the second node 1128 of the resistor R4.

[0066] The fourth sub-circuit 1114 has substantially the same configuration as the third sub-circuit 1112. The third and fourth sub-circuits 1112 and 1114 similarly have feed forward connections 1140 and 1142, respectively, to enhance device performance. The third and fourth sub-circuits 1112 and 1114 are provided in series with the first and second sub-circuits 1016 and 1028, respectively.

[0067] In addition to the above, the signal generator 1002 includes additional components to facilitate bidirectional communication, i.e., signals going from the high side device (or load) to the low side device, so that certain events may be conveyed to the circuits or devices that are connected to the low side device.

[0068] The signal generator 1002 includes a third pulse generator 1202 that is coupled to the second pulse generator 1053. A plurality of invertors 1210, 1212, and 1214 are coupled to the third pulse generator and to the comparator 1038. The invertors are arranged in two groups. One group 1213 includes the inverters 1210 and 1212 that are arranged serially. Another group 1215 includes the inverter 1214. These two groups of inverters are configured to output complementary signals.

[0069] The inverter group 1213 is coupled to a first communication circuit 1216 having an input node 1218 and an output node 1220. The input node 1218 of the circuit 1216 is

coupled to the output of the inverter 1212. The output node 1220 of the circuit 1216 is coupled to the fourth sub-circuit 814 and the first high-side node 1009a.

[0070] The first communication circuit 1216 includes a resistor R_{1H}, a capacitor C_{1H}, and a capacitor C_{SH}. The resistor R_{1H} is provided between the input and output nodes 1218 and 1220. In one implementation, the resistor R_{5H} has the substantially the same resistive value as the resister R_{4a} of the circuit 1114. The capacitor C_{1H} represents the resistor-to-substrate capacitance. The capacitor C_{SH} represents the bond-pad-to-substrate capacitance and has a potential V_{BC1H}.

[0071] A second communication circuit 1222 is coupled to the node 1218 and includes a resistor R_{5H} and a capacitor C_{5H}. One end of the resistor R_{5H} is coupled to the node 1218, and the other is coupled to the input node 1042 to the comparator 1038. The capacitor C_{5H} represents the resistor-to-substrate capacitance. The resistor R_{5H} is provided with a resistive value that is substantially the same as the combined resistive value of the resisters R_{4a} and R_{1H}.

[0072] The inverter group 1215 is coupled to a third communication circuit 1224. The circuit 1224 includes an input node 1226, an output node 1228, and a resistor R_{1aH} provided between the nodes 1226 and 1228. A capacitor C_{1aH} represents the resistor-to-substrate capacitance. A capacitor C_{SaH} represents a bond-pad-to-substrate capacitance and has a potential V_{BV1aH}.

[0073] A fourth communication circuit 1230 is coupled to the node 1226 and includes a resistor R_{5aH} and a capacitor C_{5aH}. One end of the resistor R_{5aH} is coupled to the node 1226, and the other is coupled to the input node 1040 to the comparator 1038. The capacitor C_{5aH} represents the resistor-to-substrate capacitance. The resistor R_{5aH} is provided with a resistive value that is substantially the same as the combined resistive value of the resisters R_4 and R_{1aH}.

[0074] The first, second, third, and fourth communication circuits are used to provide signals to a comparator 1250 on the low-side driver from the inverter groups 1213 and 1215 without interfering with the operations of the comparator 1038. The comparator 1250 has input nodes 1252 and 1254.

[0075] In operation, the inverter group 1213 sends a signal 1256a to the input node 1252 of the comparator 1250 via the node 1009a. The inverter group 1215 sends a signal 1258a to the input node 1254 of the comparator 1250 via the node 1009b.

[0076] The signals 1256a and 1258a are also applied to the input nodes 1040 and 1042 of the comparator 1038 on the high side, which are noise from the point of the comparator 1038. This noise is substantially reduced or eliminated by signals 1256b and 1258b that are complements of the signals 1258a and 1256a, respectively. That is, the signal 1258a and the signal 1256b, complementary signals, are input to the node 1042, thereby canceling the two signals. For this purpose, the combined resistive values of the resistors R_{1aH} and R_4 and that of the resistor R_{5H} are provided to be the same. Similarly, the signal 1256a and signal 1258b cancel each other at the node 1040.

[0077] The low-side driver also includes a plurality of circuits 1260, 1262, 1264, and 1266 that are used to provide signals to the comparator 1038 without interfering with the operations of the comparator 1250. The circuit 1260 includes a resistor R_{4a}, a capacitor C_{4a}, and a capacitor C_{scL}. The capacitor C_{scL} defines a potential V_{BVC4aL}. The circuit 1262 includes a resistor R_{4L}, a capacitor C_{4L}, and a capacitor C_{sbL}. The capacitor CsbL defines a potential of V_{BVC4L}. The circuit 1264 includes a resistor R_5 and a capacitor C_5. The circuit 1266 includes a resistor R_{5a} and a capacitor C_{5a}.

[0078] In the present embodiment, the circuits are configured to provide the following potentials:

$$V_{BVC1} \approx V_{BVC1a}$$
$$V_{BVC4} \approx V_{BVC4a}$$
$$V_{BVC1} \approx V_{BVC4}$$
$$V_{BVC1H} \approx V_{BVC1aH}$$
$$V_{BVC4L} \approx V_{BVC4aL}$$
$$V_{BVC1H} \approx V_{BVC4L}$$
$$V_{SF} + V_{CM} \leq V_{BVC1}$$

[0079] The above detailed descriptions are provided to illustrate specific embodiments of the present invention and are not intended to be limiting. Numerous modifications and variations within the scope of the present invention are possible. Accordingly, the present invention is defined by the appended claims.